In the claims:

Following is a complete set of claims as amended with this Response.

1. (Currently Amended) An apparatus comprising:

a bypass clock input to receive a bypass clock from an external source for bypass clock operation;

a reference input port to receive a reference clock, the reference clock being based alternately on an external oscillator for normal operation or on the ~~on a~~ bypass clock;

a clock selection multiplexer to select the bypass clock for bypass operation or the reference clock for normal operation;

a feedback input port to receive a feedback clock from a clocked circuit; and

logic to compare the reference clock based on the bypass clock in bypass operation and the feedback clock and to generate an output based on the comparison the output being a signal to indicate whether the reference clock and the feedback clock are aligned.

2. (Original)The apparatus of Claim 1, wherein the bypass clock is an external clock signal.

3. (Original)The apparatus of Claim 1, further comprising a clock distribution circuit to generate the feedback clock.

4. (Canceled)

5. (Original)The apparatus of Claim 1, wherein the output comprises a pulse suppression signal to suppress a portion of the bypass clock.

6. (Original)The apparatus of Claim 5, wherein the portion of the bypass clock is a single pulse of the bypass clock.

7. (Original)The apparatus of Claim 5, wherein the pulse suppression signal changes the timing of the feedback signal.

8. (Original)The apparatus of Claim 5, further comprising a bypass clock input and a gate coupled to the bypass clock input and to the pulse suppression signal to suppress a portion of the bypass clock signal in response to the pulse suppression signal.

9. (Original)The apparatus of Claim 1, further comprising a reference edge detector to receive the reference clock signal and provide a reference edge detection signal to the logic and a feedback edge detector to receive the feedback clock signal and to provide a feedback edge detection signal to the logic, and wherein the output comprises an indicator signal to indicate whether the reference edge detection signal and the feedback edge detection signal are aligned.

10. (Canceled)

11. (Original)The apparatus of Claim 1, wherein the frequency divider comprises a counter with a reset trigger to reset the reference clock in response to an external trigger signal.

12. (Currently Amended)The apparatus of Claim 1, ~~further comprising~~ wherein the clock selection multiplexer comprises a clock selector to suppress an internally synchronized clock based on the external oscillator for normal operation and substitute the bypass clock.

13. (Currently Amended)The apparatus of Claim 1, ~~wherein the output comprises an indicator signal to indicate whether the reference clock and the feedback clock are aligned, the apparatus~~ further comprising:

a second reference input port to receive the reference clock;

a second feedback input port to receive a second feedback clock from a second clocked circuit;

a second logic to compare the reference clock and the second feedback clock and to generate a second indicator signal to indicate whether the reference clock and the second feedback clock are aligned based on the second logic comparison; and

indication logic to receive the first indicator signal and the second indicator signal and to generate a combined lock indication.

14. (Original)The apparatus of Claim 13, wherein the indication logic comprises a gate to combine the first indicator signal with a first frequency signal, a second gate to combine the second indicator signal with a second frequency signal, and a third gate to combine the results of the first gate and the second gate.

15. (Original)The apparatus of Claim 1, further comprising a second clocked circuit and a phase circuit to receive the bypass clock and a second feedback clock from the second clocked circuit to generate the reference clock.

16. (Original)The apparatus of Claim 15, wherein the phase circuit comprises a phase locked loop for the second clock circuit and wherein the reference clock is applied as a clock circuit for the second clocked circuit.

17. (Currently Amended)A computer system comprising:

a voltage controlled crystal oscillator to generate a primary clock;

a phase locked loop having a first ~~phase locked loop~~ input to receive the primary clock, ~~clock;~~ a second ~~phase locked loop~~ input to receive a feedback clock from a clocked circuit, and an circuit; a phase locked loop output to generated a synchronized clock for normal operation;

a bypass gate to select one of the synchronized clock for normal operation or a bypass clock for bypass operation to apply as a timing signal for the clocked circuit; and

logic to compare a reference clock and the feedback clock and to adjust the timing of the bypass clock independent of the phase locked loop based on the comparison, wherein the reference clock is based on the bypass clock.

18. (Original)The system of Claim 17, wherein the clocked circuit is an input/output circuit to receive the bypass clock as the timing signal, the apparatus further comprising a memory controller coupled to the input/output circuit.

19. (Original)The system of Claim 17, further comprising a clock distribution circuit to generate the feedback clock from the timing signal.

20. (Original)The system of Claim 17, further comprising a frequency divider to receive the bypass clock and to generate the reference clock by dividing the bypass clock in response to a configurable ratio parameter.

21. (Original)The system of Claim 17, wherein the frequency divider comprises a counter with a reset trigger to reset the reference clock in response to an external trigger signal.

22. (Original)The system of Claim 17, wherein the logic generates a lock indicator signal to indicate whether the reference clock and the feedback clock are aligned.

23. (Original)The system of Claim 17, further comprising a second clocked circuit and a phase circuit to receive the bypass clock and a second feedback clock from the second clocked circuit to generate the reference clock.

24. (Currently Amended)A method comprising:

receiving a bypass clock from an external source for bypass clock operation;

receiving a reference clock, the reference clock being based alternately on an external oscillator for normal operation or on the ~~on a~~ bypass clock;

selecting one of the bypass clock for bypass operation or the reference clock for normal operation;

receiving a feedback clock from a clocked circuit; and

comparing the reference clock and the feedback clock in bypass operation and generating an output based on the comparison, the output being a signal to indicate whether the reference clock and the feedback clock are aligned.

25. (Canceled)

26. (Canceled)

27. (Original)The method of Claim 24, wherein generating an output comprises generating a pulse suppression signal to change the timing of the bypass signal.

28. (Original)The method of Claim 24, wherein the reference clock comprises the bypass clock divided down by a ratio determined in response to a configurable ratio parameter.

29. (Original)The method of Claim 24, further comprising receiving an external trigger signal and resetting the reference clock in response to the external trigger signal.

30. (Currently Amended)The method of Claim 24, further comprising receiving the bypass clock and a second feedback clock for a second clocked circuit at a phase locked loop for the second clocked circuit and generating a timing signal ~~the reference clock~~ at the phase locked loop.

31. (Currently Amended)The method of Claim 30, further comprising applying the timing signal ~~reference clock~~ of the phase locked loop as a timing signal for the second clocked circuit.

32. (Currently Amended)An article of manufacture comprising a machine-accessible medium including data that, when accessed by a machine, cause the machine to perform operations comprising:

receiving a bypass clock from an external source for bypass clock operation;

receiving a reference clock, the reference clock being based alternately on an external oscillator for normal operation or on the ~~on a~~ bypass clock;

selecting one of the bypass clock for bypass operation or the reference clock for normal operation;

receiving a feedback clock from a clocked circuit; and

comparing the reference clock and the feedback clock in bypass operation and generating an output based on the comparison, the output being a signal to indicate whether the reference clock and the feedback clock are aligned.

33. (Canceled)

34. (Canceled)

35. (Original)The article of Claim 32, wherein generating an output comprises generating a pulse suppression signal to change the timing of the bypass signal.

36. (Original)The article of Claim 32, wherein the reference clock comprises the bypass clock divided down by a ratio determined in response to a configurable ratio parameter.

37. (Original)The article of Claim 32, wherein the machine-accessible medium further includes data that cause the machine to perform operations comprising receiving an external trigger signal and resetting the reference clock in response to the external trigger signal.

38. (Currently Amended)The article of Claim 32, wherein the machine-accessible medium further includes data that cause the machine to perform operations comprising receiving the bypass clock and a second feedback clock for a second clocked circuit at a phase locked loop for the second clocked circuit and generating a timing signal ~~the reference clock~~ at the phase locked loop.

39. (Currently Amended)The article of Claim 38, wherein the machine-accessible medium further includes data that cause the machine to perform operations comprising applying the timing signal ~~reference clock~~ of the phase locked loop as a timing signal for the second clocked circuit.